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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/722,380	11/28/2000	Timothy J. Van Hook	723-957	4467

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EXAMINER	
NGUYEN, HAU H	
ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/722,380	Applicant(s) VAN HOOK ET AL.	
	Examiner Hau H Nguyen	Art Unit 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claim 5, 12-14, 17-19, 22-24 are rejected under 35 U.S.C. 102(a) as being anticipated by Fielder et al. (U.S. Patent No. 5,694,143).

Referring to claims 5, 14, 19, and 23, Fielder et al. teach a single chip display processor is comprised of a dynamic random access memory (DRAM) for storing at least one of graphics and video pixel data, a pixel data unit (PDU) for processing the pixel data, integrated in the same integrated circuit (IC) chip as the DRAM, the IC chip further comprising a massively parallel bus for transferring blocks of pixel data at the same time from the DRAM to the PDU, whereby the PDU can process the blocks of pixel data for subsequent display of processed pixel data (col. 3, lines 23-32). The system could allow full-motion video to be input in a variety of different standard formats, including GREY8, RGB332, RGB565, RGB555, ARGB8888, LUT8, RGB888, YUV411, YUV422 and YUV420, as well as other formats (col. 2, lines 14-17).

In regard to claims 12, 22, and 28, as cited above, Fielder et al. teach the YUV format also comprising YUV4:2:0.

In regard to claim 13, as cited above, Field et al. teach the embedded frame buffer is a DRAM.

Referring to claim 17, Fielder et al. teach the single chip graphics system utilizes a massively parallel bus, in a novel architecture. This provides an interface between the frame buffer memory and a pixel processor to be extremely wide (col. 2, lines 58-62).

In regard to claims 18 and 24, Fielder et al. teach the data of an entire line of pixels, frame or part of a frame is thereby transferred in parallel between the memory and the pixel processor, whereby the pixel processor processes each bit in parallel with the others that have been transferred (col. 1, lines 66-68, and col. 2, lines 1-3). Since the graphics system can receive data of different format, it is implied that the frame buffer is reconfigured frame-by-frame basis.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fielder et al. (U.S. Patent No. 5,694,143) in view of Grossman (U.S. Patent No. 5,307,450).

Referring to claims 1, Fielder et al. teach a frame buffer system, including the memory controller, a basic pixel processor and a pixel logic system including a RAMDAC, are integrated into a single integrated circuit chip (IC) (col. 2, lines 23-26). The system could also allow full-motion video to be input in a variety of different standard formats, including GREY8, RGB332, RGB565, RGB555, ARGB8888, LUT8, RGB888, YUV411, YUV422 and YUV420, as well as

other formats (col. 2, lines 14-17). Thus, Fielder et al. teach all the limitations of claim 1, except for a graphics pipeline.

However, graphics pipeline is well known in the art as described in U.S. Patent No. 5,307,450 ('450) to Grossman (Fig. 1).

Therefore, it would have been obvious to one skilled in the art to utilize a graphics pipeline as taught by Grossman. in the graphic system as taught by Fielder et al. in order to speed up graphics processing.

In regard to claims 2 and 3, with reference to Fig. 1, Fielder et al. teach a display processor 40 is connected to the system bus 15 via an e.g. 32 bit bus 41 and a control input (not shown in this figure) and receives digitized video signals via a 4 bit bus 42 (col. 5, lines 13-17). Video and graphics pixel data are received from the shift registers in the frame buffer on the GRAPHICS and VIDEO buses, four 8 bit pixels simultaneously, and are applied to graphics formatter 130 and video formatter 131. In the formatters the pixels are formatted to enable a stream of one pixel per cycle, and are re-timed. The resulting video signal is applied to the color space converter 33 where the video may be in a format such as YUV (col. 14, lines 66-68, and col. 15, lines 1-6). In combination with reference '450, as shown in Fig. 1, Grossman teach the graphics pipeline writes RGB color format to the frame buffer.

Referring to claim 4, Fielder et al. teach the data of an entire line of pixels, frame or part of a frame is thereby transferred in parallel between the memory and the pixel processor, whereby the pixel processor processes each bit in parallel with the others that have been transferred (col. 1, lines 66-68, and col. 2, lines 1-3). Since the graphics system can receive data of different format, it is implied that the frame buffer is reconfigured frame-by-frame basis.

5. Claims 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fielder et al. (U.S. Patent No. 5,694,143) in view of Foley and van Dam ("Computer Graphics: Principle and Practice, Second Edition) (hereinafter 'Foley').

Referring to claims 6 and 25, as cited above, Fielder et al. teach all the limitations of claim 6, except for the anti-aliasing of the image using point sampling or super-sampling. However, Foley teach a method of antialiasing using point sampling and super sampling as described on pages 619-620, wherein, in point sampling, one point for each pixel is selected, evaluate the original signal at this point, and assigned its value to the pixel (page 619, section 14.10.1). In super sampling, more than one sample for each pixel are selected and combined (page 620, section 14.10.1). Thus, anti-aliasing is used to reduce the jaggies or stair-casing (page 132, section 3.17.1).

Therefore, it would have been obvious for point sampling is used with more bit format, such 48-bit format for point sampling, or 96-bit format for super sampling as claimed, since the benefit of increasing more bits to point sampling or super sampling is to obtain a better resolution for the displayed image.

6. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fielder et al. (U.S. Patent No. 5,694,143) in view of Videum Conference Pro (PCI), products of Winnov (Winnov).

Referring to claims 15 and 16, as applied to claim 14, Fielder et al. teach all the limitations of claims 15 and 16, except for the embedded frame buffer partitioned to store 720x576 Y, 360x288 U, 360x288 V for a YUV 4:2:0 frame, and 24 color bits.

However, Winnov teaches a video conferencing PCI receiving different video formats including YUV 4:2:0, and the still image resolution having a width 720 and height 576 (PAL), and up to 1024 pixels interpolated, 24-bit colors.

Therefore, it would have been obvious to one skilled in the art to utilize the resolution as taught by Winnov in combination with the graphics system as taught by Fielder et al. in order to produce high-performance, low-cost video signals.

7. Claims 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fielder et al. (U.S. Patent No. 5,694,143) in view of Burbank (U.S. Patent No. 6,476,822).

Referring to claim 20, as cited above, Fielder et al. teach the format of input signal comprising RGB332, RGB565, RGB555, ARGB8888 (thus 24 bits for color), LUT8, RGB888, YUV411, YUV422 and YUV420, as well as other formats (col. 2, lines 14-17). Thus, Fielder et al. and Foley teach all the limitations of claim 20, except for the color depth is 24 bits.

However, Burbank teaches a method of applying 24 bits color depth (col. 1, lines 36-42).

Therefore, it would have been obvious to one skilled to utilize the 24 depth bits as taught by Burbank in combination with the graphics system as taught by Fielder et al. and Foley in order to produce true color images (col. 1, lines 39-40).

8. Claims 7-11, 21, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fielder et al. (U.S. Patent No. 5,694,143) in view of Foley and van Dam ("Computer Graphics: Principle and Practice, Second Edition) further in view of Burbank (U.S. Patent No. 6,476,822).

Referring to claims 7-8, and 26, as cited above, Fielder et al. teach the format of input signal comprising RGB888 format, thus 24 bits for color. As applied to claim 6, Fielder et al. and Foley teach all the limitations of claims 7-8, and 26, except for the color depth is 24 bits.

However, Burbank teaches a method of applying 24 bits color depth (col. 1, lines 36-42).

Therefore, it would have been obvious to one skilled to utilize the 24 depth bits as taught by Burbank in combination with the graphics system as taught by Fielder et al. and Foley in order to produce true color images (col. 1, lines 39-40).

In regard to claim 9-11, 21, and 27, as cited above, Fielder et al. teach the input format comprising RGB565 (16 bits color data), Foley teach the method of anti-aliasing using point sampling and super sampling. Thus, Felder et al. and Foley teach all the limitations of claims 9-11, except for the super sampling 96-bit format. However, it would have been obvious to one skilled in the art to use more bits per pixel for super sampling in order to obtain a better resolution for the displayed image.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892 form.

Rutman (U.S. Patent No. 5,890,190) discloses a frame buffer system is provided for displaying pixels of differing types according to standard pixel information types.

Leung (U.S. Patent No. 6,215,497) discloses a graphics sub-system having a 2-D graphics accelerator, a 3-D graphics accelerator and an embedded DRAM memory. The embedded

DRAM memory serves as a frame buffer memory and/or a temporary storage memory for the 2-D graphics accelerator.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

02/24/2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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